IN THE SPECIFICATION

Page 1, before the first line, add the paragraph:

This is a continuation of U.S. Serial No. 08/184,070, filed on January 21, 1994 (now allowed), which is a reissue of U.S. Patent No. 5,083,296, issued on January 21, 1992.

Column 2, second full paragraph (lines 19-23), replace the paragraph with:

The operation of the foregoing arrangement will be explained on the timing charts of FIGS. 2A and 2B. FIG. 2A shows the read cycle and write cycle, and FIG. 2B shows reading and writing in the page mode cycle, and the refresh cycle ~~and page mode cycle~~.

Column 3, first full paragraph (lines 5-19), replace the paragraph with:

As in the read or write cycle, a refresh address RFi is latched in the row latch in response to the clock signal CLK of the first cycle and the row decoder 3 decodes the refresh address RFi latched in the latch 2 to activate a selected one of the row lines X0-X1023, and the refresh operation starts. Subsequently, the chip select signal CS is made high before the second clock signal CLK goes high. The chip select signal

CS is disactivated when the second clock signal CLK rises, causing the column latch 4, column decoder 5 and column selection circuit 6 to quit operation, and the data input/output operation does not take place. The clock signal CLK of the ~~third~~ second cycle is a dummy for making cycles consistent with the read and write cycle, and the refresh cycle completes by using clock signals CLK of three cycles.

Column 3, fifth full paragraph (lines 50-55), replace the paragraph with:

The latch 10 has its output signal CT applied to the inverting input terminal of the two-input AND gate 14 and to the input terminals of the three-input AND gate 15. The two-input AND gate 14 produces the row address set signal RS1 and the three-input AND gate 15 produces the column address set signal CS1.